## AMENDMENTS TO THE CLAIMS:

1-35. (Cancelled)

36. (Currently Amended) The method of claim [35] 37, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug includes forming the second doped plug in the second doped well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first doped plug and the second doped plug.

37. (Currently Amended) [The method of claim 35, wherein forming the first doped plug includes forming] A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

forming a first doped plug within the first doped well, wherein the first doped plug is formed a first distance from a first boundary of the first doped well, and, wherein the first distance is selected to provide approximately a desired breakover voltage between the first doped plug and the first doped region [depends on the first distance];

forming a second doped plug into the first doped region; and

forming an isolation structure between the first and second doped plugs.

38. (Currently Amended) The method of claim [35] 37, wherein forming the isolation structure includes forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

39. (Currently Amended) The method of claim [35] 37, wherein forming the isolation structure includes forming a gate terminal.

40. (Original) The method of claim 39, wherein forming the gate terminal includes:

forming a dielectric layer adjacent to at least a portion of the first doped region; and

forming a conductor layer above at least a portion of the dielectric layer.

41. (Currently Amended) The method of claim [35] 37, further comprising forming a conductor layer above at least a portion of the first and second doped plugs.

42. (Currently Amended) The method of claim [35] 37, wherein providing the first doped region comprises providing a p-type first doped region.

43. (Currently Amended) The method of claim [35] 37, wherein forming the first and second doped plugs comprises forming n-type first and second doped plugs.

44. (Canceled.)

45. (Currently Amended) The method of claim [44] 46, further comprising forming a second n-well within the p-type semiconductor substrate, wherein forming the second n-plug within the p-type semiconductor substrate comprises forming [a] the second n-plug within the second n-well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first n-plug and the second n-plug.

46. (Currently Amended) [The method of claim 44, wherein forming the first n-plug within the first n-well comprises forming] A method comprising:

providing a p-type semiconductor substrate;

forming a first n-well within the p-type semiconductor substrate;

forming a first n-plug within the first n-well, wherein the first n-plug is formed a first distance from a first boundary of the first n-well, and wherein the first distance is selected to provide approximately a desired breakover voltage between the first n-plug and the p-type semiconductor substrate [depends on the first distance];

forming a second n-plug within the p-type semiconductor substrate; and

forming an isolation structure between the first and second n-plugs.

47. (Currently Amended) The method of claim [44] 46, wherein forming the isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

48. (Currently Amended) The method of claim [44] 46, wherein forming an isolation structure comprises forming a gate terminal.

49. (Previously Added) The method of claim 48, wherein forming a gate terminal comprises:

forming a dielectric layer adjacent at least a portion of the semiconductor substrate; and

forming a conductor layer above at least a portion of the dielectric layer.

50. (Currently Amended) The method of claim [44] 46, further comprising forming a conductor layer above at least a portion of the first and second n-plugs.

51. (Currently Amended) A method for forming an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first doped region in the semiconductor substrate;

forming a first doped well within the first doped region;

forming a first doped plug at [selected location within the first doped well] a first distance from a first boundary of the first doped well, wherein the [selected location is selected to provide] first distance is selected to provide approximately a first desired breakover voltage between the first doped plug and the first doped region;

forming a second doped plug within the first doped region;

forming an isolation structure between the first and second doped plugs;

forming a bond pad on the semiconductor substrate;

forming a voltage source node on the semiconductor substrate;

coupling the first doped plug to the bond pad;

coupling the second doped plug to the voltage source node; and

forming at least one integrated circuit component on said semiconductor substrate coupled to the bond pad.